Surface mount (smt) connector for VCSEL and photodiode arrays

Self alignment of Optoelectronic (OE) chips, such as photodiode (PD) modules and vertical cavity surface emitting laser (VCSEL) modules, to external waveguides or fiber arrays may be realized by packaging the OE chips directly in the fiber optic connector.
Description

FIELD OF THE INVENTION

[0001] Embodiments of the present invention relate to connectors and, more particularly, to surface mount connectors for optoelectronic devices.

BACKGROUND INFORMATION

[0002] With the proliferation of optical communication systems the use of small fiber optic connectors has become more prevalent. Optical connectors are typically made of plastic and are useful components for joining optical fibers or waveguide arrays at their ends. Optical connectors are typically pluggable, meaning that they may allow for repeated connection and disconnection. There are many types of optical connectors available on the market today.

[0003] Figure 1 shows an example a Mechanically Transferable or "MT"-style connector. Some also refer to "MT" as Multi-Terminal connectors. MT connectors are one type of what are known as small form factor (SFF) connectors. MT connectors are popular for parallel optical data transmission since they provide a high fiber count in a dense connector package comprising an arrayed configuration of fiber holes aligned in a single ferrule. Commercially available MT connectors may comprise anywhere from two to twenty-four connection points and in the future will likely comprise many times that number.

[0004] Referring to Figures 1 and 2 there is shown an example of an MT-style connector. Figure 1 shows a female portion 100 and a male portion 102 of the connector. Figure 2 shows a more detailed plan view of the female portion 100. A female input 101 and a male input 103 may comprise either optical fibers or waveguide arrays intended to be optically connected to each other. Both the female portion 100 and the male portion 102 hold arrays of corresponding exposed optical connection points 104 and 106 in ferrules, 108 and 110. The connection points 104 and 106 may be aligned by a pair of metal guide pins 112 at the end of the male portion 102, which join into guide holes 114 on the female portion 100. The MT connector may be locked together by a push and click mechanism or may comprise a fastener (not shown) that clips between the end 116 of the female portion 100 and the end 118 of the male portion 102.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a Mechanically Transferable or "MT"-style connector;
[0006] Figure 2 is a plan view of a female portion of an MT-style connector;
[0007] Figure 3 is a side view of optical and electrical components on a flip-chip ball grid array (FC-BGA) package;
[0008] Figure 4 is a side view of a of optical and electrical components on a flip-chip ball grid array (FC-BGA) package according to embodiments of the invention;
[0009] Figures 5A, 5B, and 5C illustrate an exemplary fabrication process for packaging an optoelectronic chip in an optical connector; and
[0010] Figure 6 is a view of optical connectors with built-in optoelectronic devices used for internal chip-to-chip optical interconnects as well as external optical interconnects.

DETAILED DESCRIPTION

[0011] Referring now to Figure 3, there is shown a side view of an optical transceiver 300 that utilizes MT-style connectors 302 and 304. As shown, a flip-chip Ball/Grid Array (FC-BGA) substrate 306 may be mounted to a printed circuit board (PCB) 308. The FC-PGA substrate 306 may have attached thereto a Complementary Metal Oxide Semiconductor (CMOS) transceiver 310 including circuitry for driving a vertical cavity surface emitting laser (VCSEL) module 312 as well as receiver circuitry for detecting signals from a photo-diode (PD) array module 314. Transceiver 310, the VCSEL module 312, and the PD module 314 may be flip-chip bonded to the FC-PGA substrate 306 via solder ball arrays 316.

[0012] A first polymer waveguide array 318 couples incoming light signals from the MT-style connector 302 to the PD module 318. The PD module 318 translates the incoming light signals into electrical signals for the transceiver 310. Likewise, electrical signals for transmission from the transceiver 310 are supplied to the VCSEL module 312. A second polymer waveguide array 320 couples light signals output by the VCSEL module 312 to the MT-style connector 304.

[0013] One end of the of each of the first and second polymer waveguide arrays, 318 and 320, are configured at a 45° angle and coated with reflective materials to form a first total internal reflection (TIR) mirror 322 and a second TIR mirror 324. This may be accomplished by cutting or slicing the waveguide array, 318 or 320, at a 45° angle using, for example, micromaching or laser ablation techniques. In this manner incoming light signals from the MT-style connector 302 travel down the first waveguide 316 and are reflected 90° upwards by the TIR mirror 322 to the PD module 314. Similarly, light emerging from the bottom of the VCSEL module 312, perpendicular to the PCB 308, are reflected at a 90° angle by the TIR mirror 324 and into the second waveguide 320 and to the MT-style connector 304. The waveguide arrays 318 and 320 should be accurately aligned to bumps on the FC-BGA substrate 306 and attached. With this configuration, visual alignment may be used for alignment of the optoelectronic chips such as VCSEL module 312 and the PD module 314.

[0014] One embodiment of the invention comprises eliminating visual alignment by packaging the optoelectronic chips such as the VCSEL module 312 or the PD module 314 directly into an MT-style connector. Figure
4 shows an optical transceiver 400 similar to the transceiver 300 shown in Figure 3 with the elimination of the waveguides 318 and 320 and TIR mirrors 322 and 324, and having the PD module 410 and the VCSEL module 414 integrated directly into the optical connectors 412 and 416, respectively.

The optical transceiver 400 of Figure 4 may comprise a FC-BGA substrate 402 on a printed circuit board 404. The FC-BGA substrate 402 may comprise a multi-layer organic substrate with multiple electric traces at each level connected by conductive vias between the layers (not shown). A CMOS transceiver 406 may be flip-chip bonded to the FC-BGA substrate 402 via solder ball array 408. The optical transceiver 400 as shown may be, for example, a high-speed, 12-channel parallel optical transceiver package and may be compatible with microprocessor package technology and at the same time allow the integration of low-cost, high-performance optical components. The CMOS transceiver 406 may be fabricated in a 0.18 μm CMOS process technology, and contain all the circuits needed for use in optical link communication such as VCSEL drivers, transimpedance amplifiers (TIAs), and limiting amplifiers (LIAs) and may form part of a central processing unit (CPU) package. While 0.18 μm CMOS process technology is offered as an example, other process technologies may also be used.

A photo-diode (PD) array module 410 may also be packaged inside of an MT-style connector to form an MT-style photo diode (PD) package 412. Similarly, a vertical cavity surface emitting laser (VCSEL) array module 414 may also be packaged inside of an MT-style connector to form an MT-style VCSEL package 416. The MT-style PD package 412 and the MT-style VCSEL package 416 may be surface mount (SMT) devices using solder ball arrays 418 and 420 to be flip chip mounted to the FC-PGA substrate 402. Conductive traces, such as those illustrated by 422 and 424, may be used to electrically connect the MT-style PD package 412 and the MT-style VCSEL package 416 to the CMOS transceiver 406.

The MT-style PD package 412 and the MT-style VCSEL package 416 may be flip-chip bonded to the FC-BGA substrate 402 via solder ball arrays 418 and 420 to be flip chip mounted to the FC-PGA substrate 402. Conductive traces, such as those illustrated by 422 and 424, may be used to electrically connect the MT-style PD package 412 and the MT-style VCSEL package 416 to the CMOS transceiver 406. The alignment marks 505 may be used to facilitate the alignment position of the OE module 414 with respect to the glass substrate 506. In one embodiment, the VCSEL array module 414 may comprise ten VCSELS illustrated by the ten apertures 508. However, the number of VCSELS in the VCSEL array module 414 may be more or less depending on the application. While a VCSEL array module 414 is discussed, this may just as easily comprise any optoelectronic chip, such as a photodiode array 410 as shown in Figure 4.

Figure 5C comprises a front view of the MT-style connector 416 shown in Figure 4, the substrate 506 may be packaged in an MT-style connector housing 416 which may comprise a generally rectangular opening 512 exposing the apertures 512. The housing 416 may comprise plastic, for example. Again, the alignment marks 505 may be used to facilitate alignment of the substrate within the housing 416. The lower row of solder bumps 504 may correspond to the solder bumps 420 on the bottom of the package for inputting and outputting electric signals and power to the array module 414. Guide holes 516 may be provided for mating guide pins (432 of Figure 4) of a complimentary MT-style connector 428.

Figure 6 illustrates embodiments of the present invention used for chip-to-chip optical interconnect such as may be used in a central processing unit (CPU) package. Here, two or more chips 600 and 602 may reside on a common board or package 604. The first chip 600 may include a transceiver 606 electrically connected by a trace 608 to a connector 610 having a built-in VCSEL array module 612. Similarly, the second chip 602 may comprises a connector 614 having a built-in photo-diode (PD) array module 616 electrically connected by trace 618 to a transceiver 620. In this manner a chip-to-chip optical interconnect may be realized using a fiber optic
connector cord, such as male-male connector 622.

Optionally each chip 600 and 602 may also include complimentary transceiver components. For example, in one embodiment chip 600 may include a PD array module 630 built into a connector 632 to receive external optical signals from another chip (not shown) within the package 604 or from an external source such as an external chip or peripheral 635, such as a memory or router. Likewise, the chip 602 may include a VCSEL array module 640 built into a connector 642 to transmit optical signals 644 to another chip within the package 604 or residing in an external chip or peripheral device 646.

According to embodiments of the invention, coupling light from/to optoelectronic components is facilitated since the optic axis of the optoelectronic components and fiber or waveguide arrays can be easily aligned. By packaging the optoelectronic module within the connector, direct coupling is possible instead of using other aids such as mirrors. Excess loss resulting from the turning mirrors may be eliminated at both transmitter and receiver interfaces resulting in the reduction of the optical loss budget of the system. Further, embodiments of the invention may be compatible with high volume manufacturing (HVM) since alignment and assembly of the OE module and the glass substrate may be done at the wafer level.

The above description of illustrated embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications can be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

The following section of the description consists of numbered paragraphs simply providing statements of the invention already described herein. The numbered paragraphs in this section are not claims. The claims are set forth below in the later section headed “Claims”.

1. An apparatus, comprising:
   at least a first optical connector; and
   an optoelectronic module housed within the first optical connector.

2. The apparatus as recited in 1, wherein the optoelectronic component comprises a vertical cavity surface emitting laser (VCSEL).

3. The apparatus as recited in 1 wherein the optoelectronic component comprises a photo-diode (PD).

4. The apparatus as recited in 1 further comprising:
   solder bumps on a surface of the optical connector to flip-chip mount the connector to a board.

5. The apparatus as recited in 1 further comprising:
   a second optical connector;
   a second optoelectronic module housed within the second optical connector; and
   a fiber optic connecting cord connecting the first optical connector and the second optical connector.

6. An optical connector, comprising:
   a substrate;
   a first set of solder bumps on the substrate a second set of solder bumps at a bottom edge of the substrate electrically connected to the first set of solder bumps;
   an optoelectronic device flip-chip bonded to the first set of solder bumps;
   an optical connector housing encasing the substrate; and
   solder bumps on a bottom of the optical connector electrically connected to second set of solder bumps.

7. The optical connector as recited in 6, further comprising: alignment holes within the optical connector housing to mate with alignment pins from a complimentary optical connector.

8. The optical connector as recited in 6 wherein the substrate comprises glass.

9. The optical connector as recited in 6 wherein the optoelectronic component comprises a vertical cavity surface emitting laser (VCSEL) array module.

10. The optical connector as recited in 6 wherein the optoelectronic component comprises a photodiode (PD) array module.

11. The optical connector as recited in 6 wherein the optical connector housing comprises a mechanically transferable (MT) connector.

12. A system comprising:
   a laser packaged within a first optical connector housing mounted to a first electronic chip;
a photodiode packaged within a second optical connector housing mounted to a second electronic chip; and
an optical fiber cord having a complimentary optical connectors at either end to mate with the first optical connector housing and the second optical connector housing to optically connect the first electronic chip to the second electronic chip.

13. The system as recited in 12, further comprising:
transmitter circuitry electrically connected to the laser; and
receiver circuitry electrically connected to the photodiode.

14. The system as recited in 13, wherein the first electronic chip and the second electronic chip comprise part of a central processing unit (CPU) package.

15. The system as recited in 13 wherein the first electronic chip resides in a peripheral module.

16. The system as recited in 13 wherein the second electronic chip resides in a peripheral module.

17. The system as recited in 16, wherein in the peripheral module comprises a memory.

18. A method, comprising:
housing a laser in a first surface mount (SMT) connector;
flip-chip bonding the first SMT connector to a first electronic chip;
housing a photodiode (PD) in a second SMT connector;
flip-chip bonding the second SMT connector to a second electronic chip;
optically connecting the first electronic chip with the second electronic chip via an optical cord plugged into the first SIVIT connector and the second SMT connector.

19. The method as recited in 18 wherein the first electronic chip and the second electronic chip reside in a central processing unit (CPU) package.

20. The method as recite in 18 wherein the first electronic chip wherein the first electronic chip resides in an electronic package and the second electronic chip resides in a peripheral device.

21. The method as recited in 18 wherein the second electronic chip resides in an electronic package and the second electronic chip resides in a peripheral device.

Claims

1. A system comprising:
a laser packaged within a first optical connector housing mounted to a first substrate and electrically coupled to a first electronic chip, the optical connector housing being plastic and shaped as a mechanically transferable type (MT-type) connector;
solder bumps on the first optical connector housing for making flip-chip connections to the first substrate;
a photodiode packaged within a second optical connector housing mounted to a second substrate and electrically coupled to the second substrate;
solder bumps on the second optical connector housing for making flip-chip connections to the second substrate; and
an optical fiber cord having complimentary optical connectors at either end to mate with the first optical connector housing and the second optical connector housing to optically connect the laser to the photodiode.

2. The system as recited in claim 1, further comprising:
transmitter circuitry electrically connected to the laser; and
receiver circuitry electrically connected to the photodiode.

3. The system as recited in claim 2 wherein the first electronic chip resides in a peripheral module.

4. The system as recited in claim 2 wherein the second electronic chip resides in a peripheral module.

5. The system as recited in claim 4, wherein in the peripheral module comprises a memory.

6. A method, comprising:
housing a laser in a first surface mount (SMT) connector;
flip-chip bonding the first SMT connector to a first substrate electrically coupled to a first electronic chip;
housing a photodiode (PD) in a second SMT connector;
flip-chip bonding the second SMT connector to a second electronic chip;
optically connecting the first electronic chip with the second electronic chip via an optical cord plugged into the first SIVIT connector and the second SMT connector.
the second electronic chip via an optical cord plugged into the first SMT connector and the second SMT connector.

7. The method as recited in claim 6 wherein the first electronic chip and the second electronic chip reside in a central processing unit (CPU) package.

8. The method as recited in claim 6 wherein the first electronic chip resides in an electronic package and the second electronic chip resides in a peripheral device.

9. The method as recited in claim 6 wherein the second electronic chip resides in an electronic package and the second electronic chip resides in a peripheral device.

10. The method as recited in claim 6 wherein the first substrate and the second substrate are the same substrate.
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**The present search report has been drawn up for all claims**

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**Examiner:** A. Jacobs
ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO. EP 10 18 3548

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on 29-10-2010. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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