Method for controlling read-out or write-in of semiconductor memory device and apparatus for the same.

A method for controlling the read-out or write-in of a semiconductor memory device, and an apparatus for the same, comprising, in the selection of memory cells in the memory cell array to read out or write in data, the steps of selecting the memory cells of a specific address in the memory cell array, accessing the memory cells of the specific address, and then and only then accessing the memory cells of the designated address corresponding to address signals input from the outside.
BACKGROUND OF THE INVENTION

Field of the Invention
The present invention relates to a method for controlling read-out or write-in of a semiconductor memory device and an apparatus for the same.

Description of the Prior Art
The characteristics, for example, working velocity, of a semiconductor memory device, especially a random access memory (RAM), depend on the selection pattern since the memory cells are selected at random in such a device.

Therefore, in the preshipment test, various selection patterns are used for testing, those characteristics in a RAM, each cell of the memory cell array is directly selected by a corresponding address command.

For example, if a plurality of cells a, b, c, d, e are to be selected, the selection pattern may be "a → b → c → d → e", "a → b → e → c → d → e", etc. Such differences in the patterns by which memory cells are selected result in different characteristics of the semiconductor memory device.

In the prior art, compliance with the required working characteristics at all such selection patterns had to be confirmed by testing with all the selection patterns, thus requiring an extremely long testing time.

SUMMARY OF THE INVENTION
An object of the present invention is to provide a method by which the dependence of the working characteristics of a semiconductor memory device on the selection patterns of the memory cells is reduced and in which the testing of the semiconductor memory device is facilitated. Another object of the present invention is to provide an apparatus for the same.
The above-mentioned first object can be achieved by a method for controlling the read-out or write-in of a semiconductor memory device comprising, in the selection of memory cells in the memory cell array to read out or write in data, the steps of selecting the memory cells of a specific address in the memory cell array, accessing the memory cells of the specific address, and then and only then accessing the memory cells of the designated address corresponding to address signals input from the outside.

The above-mentioned second object of the present invention can be obtained by an apparatus for controlling the read-out or write-in of a semiconductor memory device, wherein an address latch portion, an address decoder portion, a memory cell array portion, and an output latch portion are formed. The address latch portion receives as input an address latch clock, an address of a cell to be selected in the memory cell array portion, and a fixed address setting signal FAS for setting the fixed address corresponding to a cell to be specified in the memory cell array portion. It generates the address of the cell to be selected between downedges of the clock and the fixed address of the cell to be specified on both sides of the downedge of clock. The address decoder portion decodes the address SA and the address FA into a decoded address DSA and a decoded address DFA, respectively. The memory cell array portion outputs data ds and data df stored in the decoded address DSA and the decoded address DFA, respectively. The output latch portion 5 latches only the data ds.

Further features and advantages of the present invention will be apparent from the ensuing description with reference to the accompanying drawings, to which, however, the scope of the invention is in no way limited.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram for explaining the method and apparatus in accordance with the present invention;

Fig. 2 is a timing chart of the block diagram of
Fig. 1;

Fig. 3 is a circuit diagram of an apparatus based on Fig. 1;

Fig. 4 is a circuit diagram of an address gate portion of the apparatus of Fig. 3;

Fig. 5 is a circuit diagram of a modification of the apparatus of Fig. 3;

Fig. 6A is an explanatory drawing of the effect in the prior art; and

Fig. 6B is an explanatory drawing of the effect in the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figs. 1 and 2, reference numeral 1 shows an address latch portion, 2 an address gate decoder portion, 3 memory cell array portion, 4 a sense amplification portion, and 5 an output latch portion.

An address latch clock ACL, an address A₀ of a cell to be selected, in the memory cell array portion, and a fixed address setting signal FAS for setting the fixed address corresponding to a cell to be specified in the memory cell array portion are input to the address latch portion 1. The address latch portion 1 outputs an address SA of the cell to be selected and a fixed address FA of the cell to be specified.

The address gate decoder portion 2 decodes the selected cell address SA and specified cell address FA and sends decoded signals DSA and DFA to the memory cell array portion 3 (see (e) in Figs. 1 and 2).

The memory cell array portion 3 reads out the data ds and df stored in cells corresponding to the above decoded signals DSA and DFA. The sense amplification portion 4 amplifies the data ds and df.

The output latch portion 5 latches by an output latch clock OCL only the data ds stored in the selected cell and generates data as shown in Fig. 1 (h) or Fig. 2 (h).

The operation of each portion in Fig. 1 will be explained hereafter referring to Figs. 3 and 4.
The address latch portion 1 consists of three parts 1a, 1b, and 1c, in which the addresses A₀, A₁, and A₂ are input respectively, as shown in Fig. 4. As all the parts of the address latch portion 1 operate the same, only the operation of part 1a will be referred to.

While the address latch clock ACL is at the "H" level, the previous state is kept. The reference will be made to Fig. 3 where the "H" leveled ACL is applied to the base of a transistor Q₁₂. The base potential of a current switch T₁₁ is higher than that of a current switch T₁₂. Therefore, current switches T₁₁ turn on, but current switches T₁₂ turn off in an input gate circuit IG. Under these circumstances, when the address A₀ is applied, since the switch T₁₉ is off the lower terminal of a resistor R₁₁ is at the "H" level.

Thus, the address SA is sent to the address gate decoder portion 2 from this part 1a as shown by (d) of Fig. 3 or in Fig. 2 (d).

On the other hand, in spite of the application of the address A₀, when the fixed address setting signal FAS is input, since the switch T₁₅ is on, a current goes through a resistor R₁₂ to the switches T₁₅ and T₁₁. Therefore, as the lower terminal of the resistor R₁₂ turns to the "L" level and the lower terminal of the resistor R₁₁ turns to the "H" level, the fixed address FA is sent to the address gate decoder portion 2, as shown by (d) of Fig. 3 or in Fig. 2 (d).

That is to say, for each downedge of the clock ALC as shown in Fig. 2 (a), the selected address A₀ and the fixed address setting signal FAS are applied to the part 1a, as shown in Figs. 2 (b) and (c). The above A₀ and FAS are latched as the output as shown in Fig. 2 (d), whereby the address A₀ between the one edge and the other edge of the clock ALC and the address FA on both sides of the downedge of the clock ALC, appear sequentially, as shown in Fig. 2 (d).

Details of the address gate decoder portion 2 are shown in Fig. 4. The two outputs of the part 1a are
applied to the bases of multiemitter transistors \( T_{21} \) and \( T_{22} \) of the address gate decoder portion 2, respectively. Emitters of the transistors \( T_{21} \) and \( T_{22} \) are connected with lines 1 to 8.

The other parts lb and lc should be also the same as the part la.

Each of lines 1 to 8 is clamped to the "H" level when an "H" level signal is applied to even one line. In the case of the embodiment of Fig. 4, an "H" level signal is applied to at least one of lines 1 to 7 and an "L" level signal is applied to only line 8, thus, each of lines 1 to 7 is clamped to the "H" level and only line 8 is clamped to the "L" level. Line 8 is connected to the base of a transistor \( Q_{21} \), and the other lines 1 to 7 are connected, respectively, to bases of the same type of transistors as transistor \( Q_{21} \), whose illustration is omitted to simplify Fig. 4. Eight signals formed by three addresses \( A_0, A_1, \) and \( A_2 \) are decoded through a line \( \text{Ⓐ} \) by a known method.

With respect to part la, the decoded signals DSA and DFA are sent to the memory cell array portion 3 as shown in (e) of Fig. 4 and Fig. 2 (e). If another three addresses \( A_3, A_4, \) and \( A_5 \) exist, these are decoded through another line \( \text{Ⓑ} \) by other parts in the same way as above.

Referring to Fig. 3, the memory cell array portion 3 consists of cells forming \( m \) columns and \( n \) rows. The data \( ds \) and \( df \) stored in the cells corresponding to the input addresses DSA and DFA (see (e) of Fig. 3 and Fig. 2 (e)) are read out as shown in (f) of Fig. 3 and Fig. 2 (f). The data \( ds \) and \( df \) are amplified by transistors \( T_{41} \) and \( T_{42} \) of the sense amplification portion 4 and are sent to the output latch portion 5.

Usually "H" levelled output latch clock OLC is applied to the base of a transistor \( T_{56} \) in the output latch portion 5, as shown in (g) of Fig. 3 and Fig. 2 (g). When OLC becomes the "L" level, a current switch \( T_{51} \) turns off, but
another current switch \( T_{52} \) turns on. As an "H" level signal is applied to the base of a transistor \( T_{53} \), but an "L" level signal is applied to the base of a transistor \( T_{57} \), the transistor \( T_{57} \) turns off and the lower terminal of a resistor \( R_{51} \) becomes the "H" level. The result is that the amplified "H" levelled data \( ds \) is output on an output transistor \( T_{54} \), as shown in (h) of Fig. 3 and Fig. 2 (h). In this manner, the function of OCL enables the output latch portion 5 to latch not the data \( df \), but the data \( ds \) stored in the memory cell array portion 3.

Figure 5 refers to a modification of the embodiment of this invention.

After the address \( A_0 \) is input, the fixed address is sent to an input gate circuit \( IG \) by turning to the "H" level the fixed address setting signal \( F \).

The operation thereafter is the same as that of part la in Fig. 3 and will therefore be deleted.

The effect of this invention will be explained hereafter based on Fig. 6B, compared with the effect of the prior art as shown in Fig. 6A.

According to the prior art, cells a, b, c, d, and e are alternatively selected as shown in arrows 1, 2, 3, and 4 or as shown in arrows 1, 2', 2", 3, and 4. But in accordance with the present invention, after the cell a is selected, the specified cell FC having the fixed address is selected (see arrow 1), after the cell FC, the cell b is selected (see arrow 2) and the cell FC is selected again (see arrow 2'). In this way, the specified cell FC is selected always between the cells a and b, b and c, c and d, d and e.

Therefore, according to this invention, as the cells a, b, c, d, and e are always selected through the specified cell FC, the dependence of the working characteristics of the memory device on the selection pattern of the memory cells is reduced. Moreover, as all the selection patterns are tested by accessing all cells during each access, the efficiency of the test of the memory device is improved.
CLAIMS

1. The above-mentioned first object can be achieved by a method for controlling the read-out or write-in of a semiconductor memory device comprising, in the selection of memory cells in the memory cell array to read out or write in data, the steps of selecting the memory cells of a specific address in the memory cell array, accessing the memory cells of the specific address, and then and only then accessing the memory cells of the designated address corresponding to address signals input from the outside.

2. An apparatus for controlling the read-out or write-in of a semiconductor memory device, wherein an address latch portion (1), an address decoder portion (2), a memory cell array portion (3), and an output latch portion (5) are connected in order;

   said address latch portion (1) receiving as input an address latch clock ACL, an address of a cell to be selected in said memory cell array portion 3 and a fixed address setting signal FAS for setting the fixed address corresponding to a cell to be specified in said memory cell array portion (3) and generating as output the address SA of the cell to be selected between downedges of the clock ACL and the fixed address FA of the cell to be specified on both sides of the downedge of the clock ACL;

   said address decoder portion (2) which decode said address SA and said address FA into a decoded address DSA and a decoded address DFA, respectively;

   said memory cell array portion (3) comprises means outputting data ds and data df stored in said decoded address DSA and said decoded address DFA, respectively; and

   said output latch portion (5) latching only said data ds.
Fig. 1

[Diagram of a circuit with labeled parts: ALC FAS, ADDRESS LATCH PORTION, ADDRESS GATE PORTION, MEMORY CELL ARRAY PORTION, SENSE AMPLIFICATION PORTION, OUTPUT LATCH PORTION, and data flow labeled (a) to (h)]
**EUROPEAN SEARCH REPORT**

**DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document with indication, where appropriate, of relevant passages</th>
<th>Relevant to claim</th>
<th>CLASSIFICATION OF THE APPLICATION (Int. Cl. ?)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>DE - A1 - 2 942 741 (LICENTIA) 1,2</td>
<td></td>
<td>G 11 C 7/00</td>
</tr>
<tr>
<td></td>
<td>* Claims 1-3; page 10, line 22 - page 12, line 1 *</td>
<td></td>
<td>G 11 C 8/00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>G 06 F 3/00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>G 06 F 13/00</td>
</tr>
<tr>
<td>A</td>
<td>DE - B2 - 2 855 744 (SIEMENS) 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Fig. *</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>DE - A1 - 2 853 926 (PHILIPS') 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Claim 1; page 11, line 30 - page 12, line 35; fig. 1,2 *</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>DE - A1 - 2 807 616 (SIEMENS) 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Claim 1; page 4, line 18 - page 5, line 13; fig. 1 *</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>DE - A1 - 2 803 989 (NCR) 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Claims 1,7 *</td>
<td></td>
<td>G 11 C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>G 06 F</td>
</tr>
<tr>
<td>A</td>
<td>US - A - 4 240 139 (FUKUDA) 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Abstract *</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>US - A - 4 086 662 (ITOH) 1,2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>* Abstract; column 2, line 49 - column 3, line 3; fig. 1,14 *</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The present search report has been drawn up for all claims

**Place of search**  | **Date of completion of the search** | **Examiner**
---|---|---
VIENNA | 22-03-1983 | NEGWER

**CATEGORY OF CITED DOCUMENTS**

<table>
<thead>
<tr>
<th>X:</th>
<th>Y:</th>
<th>A:</th>
<th>O:</th>
<th>P:</th>
</tr>
</thead>
<tbody>
<tr>
<td>particularly relevant if taken alone</td>
<td>particularly relevant if combined with another document of the same category</td>
<td>technological background</td>
<td>non-written disclosure</td>
<td>intermediate document</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T:</th>
<th>E:</th>
<th>D:</th>
<th>L:</th>
<th>&amp;:</th>
</tr>
</thead>
<tbody>
<tr>
<td>theory or principle underlying the invention</td>
<td>earlier patent document, but published on, or after the filing date</td>
<td>document cited in the application</td>
<td>document cited for other reasons</td>
<td>member of the same patent family, corresponding document</td>
</tr>
</tbody>
</table>